REMARKS/ARGUMENTS

Claims 48-62 are pending in the application. Claims 48-61 stand rejected as being unpatentable under 35 U.S.C. § 103(a) over United States Patent No. 5,346,838 to Ueno (Ueno) in view of United States Patent No. 4,861,731 to Bhagat (Bhagat).

The present application relates to forming a thyristor including a gated diode by gating a semiconductor junction with a polysilicon gate. Page 10, lines 10-15. The polysilicon gate is biased (Page 11, line 15) to produce latch up (Page 12, line 8).

In view of the above, claim 48 recites:

> A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising the following steps: providing a semiconductor substrate; providing doped silicon regions to form a multi-region planar thyristor having at least four regions; forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode; and connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor.

The pending Office Action suggests that the combination of the Ueno reference with the Bhagat reference would render the claimed invention obvious to one of ordinary skill in the art. The Office Action expressly acknowledges that Ueno does not disclose "forming at least one polysilicon gate overlying a single junction," but suggests that Ueno may be combined with Bhagat to remedy this deficiency.

The proposed combination, however, is not supported by the prior art. In order to combine references to support a rejection under 37 C.F.R. § 103(a) there must be found a motivation or suggestion in the prior art to make the combination.

The references now of record teach directly away from combining Bhagat with Ueno. The Ueno reference relates to a device having a semiconductor body including "a p-type substrate of a high impurity concentration functioning as an anode region 11. " Column 7, lines 30-31. This is shown in Fig. 3 as a back contact A.

In contrast, the Bhagat reference relates to a semiconductor power device. A "buried dielectric layer 22 defines electrically isolated thyristor cell 24." Column 4, lines 1-2. This structure is shown in Figures 1 and 2 in which dielectric layer 22 surrounds the balance of the Bhagat device, and isolates it from the substrate 20. The presence of the dielectric layer 22 of Bhagat precludes the use of a back contact as shown in Fig. 3 of the Ueno reference. A structure combining the features of the Bhagat and Ueno devices would be inoperative, since no back contact could be made through the Bhagat dielectric layer. This fundamental incompatibility between the Ueno and Bhagat devices teaches away from the combination suggested in the Office Action. Accordingly, there is no suggestion or motivation to combine the substance of the Ueno reference with that of Bhagat. Therefore, the rejection of claim 48 under 35 U.S.C. § 103(a) over Ueno in view of Bhagat should be withdrawn, and claim 48 should be allowed.

Claims 49-54 each depend, directly or indirectly, from claim 48 and incorporate every limitation thereof. Accordingly, the rejections of claims 49-54 under 35 U.S.C. § 103(a) over Ueno in view of Bhagat should be withdrawn for the same reasons given above with respect to claim 48.

Claim 55 recites:

> A method of forming a device for storing information as one of at least two possible stable current states, the method comprising the following steps: providing a semiconductor substrate; providing doped silicon regions to form a multi-region plan thyristor having at least four regions; forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode, said gate adapted

to receive a voltage for producing latch-up in said multi-region planar thyristor.

As discussed above with respect to claim 1, the Office Action acknowledges that Ueno does not teach or suggest "forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode." As further discussed above, while the Office Action relies on the Bhagat reference to remedy this deficiency, such reliance is misplaced. The substance of the Ueno and Bhagat references teaches away from the combination of Ueno with Bhagat, and consequently there is no teaching or suggestion to combine the references. Accordingly, the rejection of claim 55 under 35 U.S.C. § 103(a) over Ueno in view of Bhagat should be withdrawn for the same reasons given above with respect to claim 55.

New claim 62 has been added to more clearly define the invention. New claim 62 is believed to be immediately allowable for the reasons discussed above, and for other reasons, including the absence in the prior art of a teaching of "a method of forming a circuit for storing information as one of at least two possible stable current states."

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: April 9, 2002

Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
Michael Bergman
Registration No.: 42,318
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant